PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

3 / Prel. Amdt. A
E. Willis
11-15-01

In re the Application of

Nobuaki HASHIMOTO

Application No.: US National Stage of PCT/JP00/06824

Filed: May 24, 2001 Docket No.: 109609

For: INTERCONNECT SUBSTRATE, SEMICONDUCTOR DEVICE, METHODS OF FABRICATING, INSPECTING, AND MOUNTING THE SEMICONDUCTOR DEVICE, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 6, lines 1-3, delete current paragraph and insert therefor:

A1

(15) In this semiconductor device, the interconnect substrate may be used as the substrate.

IN THE CLAIMS:

Please replace claims 10-12 and 16-20 as follows:

A2

10. (Amended) The interconnect substrate as defined in claim 7, wherein a plurality of holes are formed in the end parts.